What is claimed is:

1. A semiconductor memory device comprising:

a first bit line for transferring data;

a second bit line having a relationship of complementary levels with the first bit line;

a storage section in which a drain electrode of a first transistor and a gate electrode of a second transistor are connected to each other to form a first node, and a drain electrode of the second transistor and a gate electrode of the first transistor are connected to each other to form a second node;

a p channel type third transistor capable of connecting the first node to the first bit line in accordance with a voltage level of a word line;

a p channel type fourth transistor capable of connecting the second node to the second bit line in accordance with the voltage level of the word line; and

a power supply circuit capable of supplying a voltage set on the condition that a difference between a source potential applied to each of the first and second transistors and a potential of a select level of the word line becomes greater than or equal to a threshold voltage of each of the third and fourth transistors, to a source electrode of each of the first and second transistors,

wherein the third and fourth transistors are configured as a vertical structure, the third transistor

is laminated over the first transistor, and the fourth transistor is laminated over the second transistor.

2. The semiconductor memory device according to claim 1, wherein the potential of the select level of the word line is set as a ground level.

3. The semiconductor memory device according to claim 2,

wherein the power supply circuit includes:

a fifth transistor connected to the source electrodes of the first and second transistors and ground; and

an error amplifier for determining a difference between a reference voltage supplied thereto and the source potential applied to each of the first and second transistors and controlling on resistance of the fifth transistor, based on the difference.

4. A semiconductor memory device comprising:

a first memory cell area in which first memory cells are disposed in an array form;

a second memory cell area in which second memory cells different in structure from the first memory cells are disposed in an array form; and

a peripheral circuit shared between the first memory cell area and the second memory cell area,

wherein said each first memory cell includes:

a storage section comprising an n channel type first MOS transistor and an n channel type second MOS transistor connected to each other;

a p channel type third MOS transistor capable of connecting a drain electrode of the first MOS transistor and a gate electrode of the second MOS transistor to a first bit line; and

a p channel type fourth MOS transistor capable of connecting a drain electrode of the second MOS transistor and a gate electrode of the first MOS transistor to the first bit line,

wherein the third and fourth MOS transistors are configured as a vertical structure, the third MOS transistor is laminated over the first MOS transistor, and the fourth MOS transistor is laminated over the second MOS transistor,

wherein said each second memory cell includes, a storage section in which a first inverter comprising a p channel type fifth MOS transistor and an n channel type sixth MOS transistor both connected in series, and a second inverter comprising a p channel type seventh MOS transistor and an n channel type eighth MOS transistor both connected in series are connected in a loop form, and

wherein the fifth and seventh MOS transistors are configured as a vertical structure, the fifth MOS

transistor is laminated over the sixth MOS transistor, and the seventh MOS transistor is laminated over the eighth MOS transistor.

5. The semiconductor memory device according to claim 4, wherein an array pitch between adjacent bit lines in the first memory cell array and an array pitch between adjacent bit lines in the second memory cell array are rendered equal to each other to share the bit lines between the first memory cell array and the second memory cell array.

6. The semiconductor memory device according to claim 4, wherein when the bit line array pitches are different from each other between the first memory cell array and the second memory cell array, a selector for selectively connecting the bit lines is interposed between the bit lines of the first memory cell array and the bit lines of the second memory cell array.

7. The semiconductor memory device according to any one of claims 1 to 6, wherein each of the third and fourth MOS transistors is set so as to retain data on the high level side in the storage section in a state in which a potential opposite in polarity to a potential for turning on a channel is being applied between a gate and source thereof.

8. A semiconductor memory device comprising:

a memory cell provided at a point where a word line and bit lines intersect;

a column selection switch for selectively connecting the bit lines to a data line;

a bit line precharge circuit for precharging each of the bit lines to a predetermined level; and

high voltage precharge means capable of precharging the bit line selected by the column selection switch at a voltage of a level higher than a precharge voltage outputted by the bit line precharge circuit.

9. The semiconductor memory device according to claim 8, further including a write amplifier connected to the bit lines via the column selection switch and capable of writing data into the corresponding memory cell through the bit line selected by the column selection switch, said write amplifier including the high voltage precharge means.

10. The semiconductor memory device according to claim 8 or 9,

wherein the memory cell includes:

a storage section comprising an n channel type first MOS transistor and an n channel type second MOS transistor connected to each other;

a p channel type third MOS transistor capable of connecting a drain electrode of the first MOS transistor and a gate electrode of the second MOS transistor to a first bit line; and

a p channel type fourth MOS transistor capable of connecting a drain electrode of the second MOS transistor and a gate electrode of the first MOS transistor to the first bit line, and

wherein the third and fourth MOS transistors are configured as a vertical structure, the third MOS transistor is laminated over the first MOS transistor, and the fourth MOS transistor is laminated over the second MOS transistor.

11. The semiconductor memory device according to claim 10, further including a power supply circuit capable of supplying a voltage set on the condition that a difference between a source potential applied to each of the first and second MOS transistors and a potential of a select level of the word line becomes greater than or equal to a threshold voltage of each of the third and fourth MOS transistors, to a source electrode of each of the first and second MOS transistors.

12. The semiconductor memory device according to claim 11, wherein each of the third and fourth MOS transistors is set so as to retain data on the high level

side in the storage section in a state in which a potential opposite in polarity to a potential for turning on a channel is being applied between a gate and source thereof.

13. A semiconductor integrated circuit comprising:

an input circuit for fetching data;

an internal logic for effecting a logical operation on the data fetched via the input circuit; and

a memory referred upon the logical operation of the internal logic,

wherein the memory includes a semiconductor memory device described in any one of claims 8 to 12, and

wherein MOS transistors identical in type to high-withstand MOS transistors used in the input circuit or output circuit are used at points where the voltage of the level higher than the precharge voltage outputted by the precharge circuit is used.